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(52) UK CL (Edition N)
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GB 2261750 A GB 2132382 A EP 0272397 A2
US 4780814 A

(58) Field of Search
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INT CL[6] B07C 1/00 9/00 , B43M 3/04 , G05B 15/02 , G06F 19/00
ONLINE DATABASES : WPI

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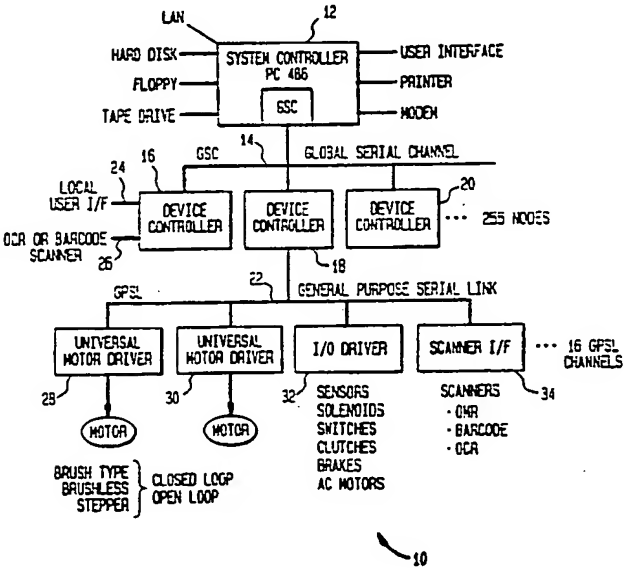
(54) System architecture for control applications

(57) A system for controlling the motors in a mail handling device includes a device control board 16, 18, 20 which communicates with a universal motor drive control board 28, 30 via a serial master-slave communication link 22 and with a system control 12 via another communication system 14 eg a GSC. The device control board is operative to receive the information for controlling the various motors from the system controller. The result is a highly flexible arrangement wherein the system blocks can be easily combined for most custom arrangements for control of mailing processes without costly development time and a necessity of maintaining a large inventory of custom boards.

FIG. 1



GB 2 283 836 A

FIG. 1

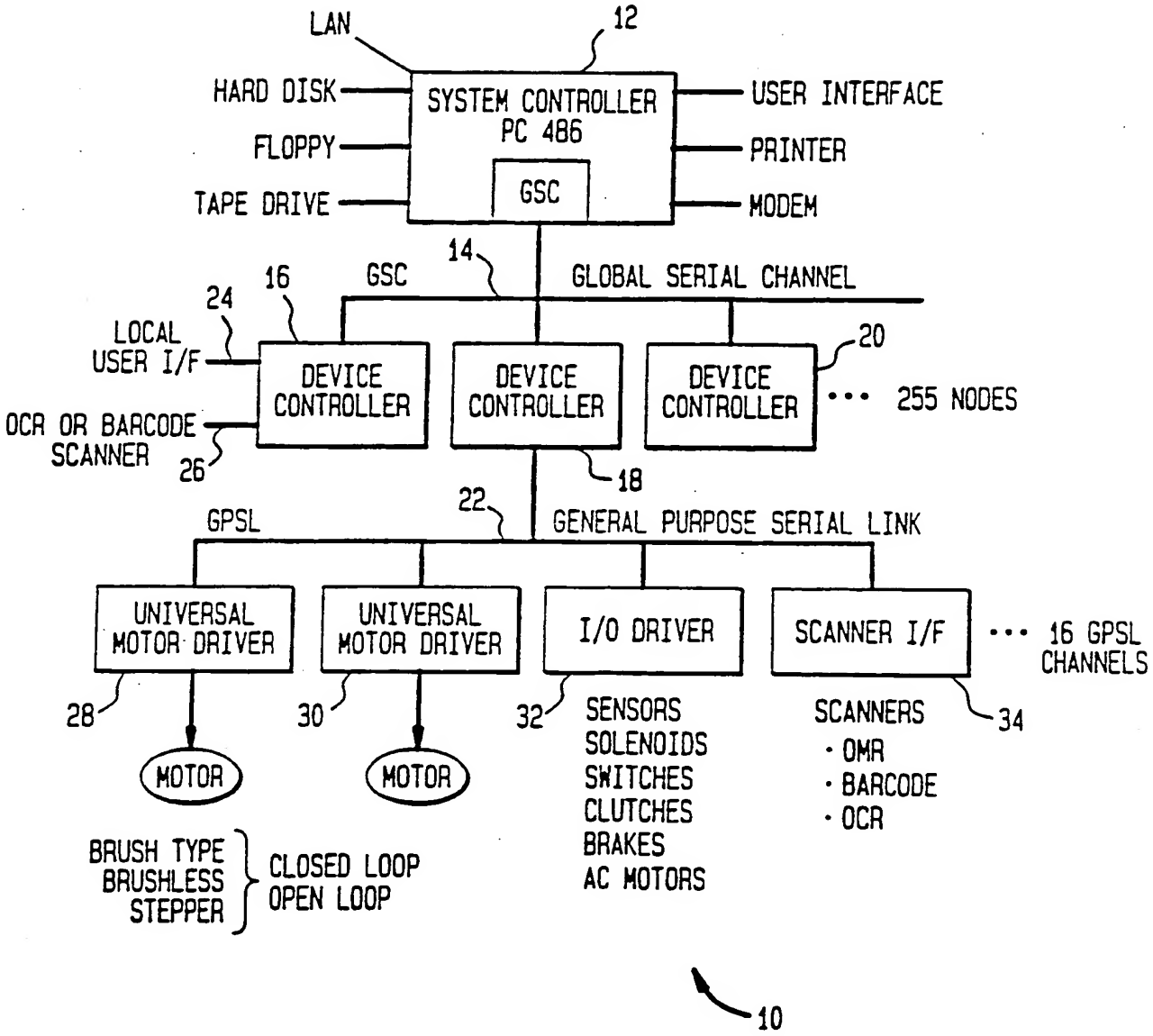

LAN
12
HARD DISK
FLOPPY
TAPE DRIVE
SYSTEM CONTROLLER
PC 486
GSC
USER INTERFACE
PRINTER
MODEM
14
GSC
GLOBAL SERIAL CHANNEL
16
24
LOCAL
USER I/F
OCR OR BARCODE
SCANNER
26
DEVICE
CONTROLLER
DEVICE
CONTROLLER
DEVICE
CONTROLLER
20
255 NODES
18
22
GPSL
GENERAL PURPOSE SERIAL LINK
UNIVERSAL
MOTOR DRIVER
UNIVERSAL
MOTOR DRIVER
I/O DRIVER
SCANNER I/F
16 GPSL
CHANNELS
28
30
32
34
MOTOR
MOTOR
BRUSH TYPE
BRUSHLESS
STEPPER
CLOSED LOOP
OPEN LOOP
SENSORS
SOLENOIDS
SWITCHES
CLUTCHES
BRAKES
AC MOTORS
SCANNERS
· OMR
· BARCODE
· OCR
10

FIG. 2

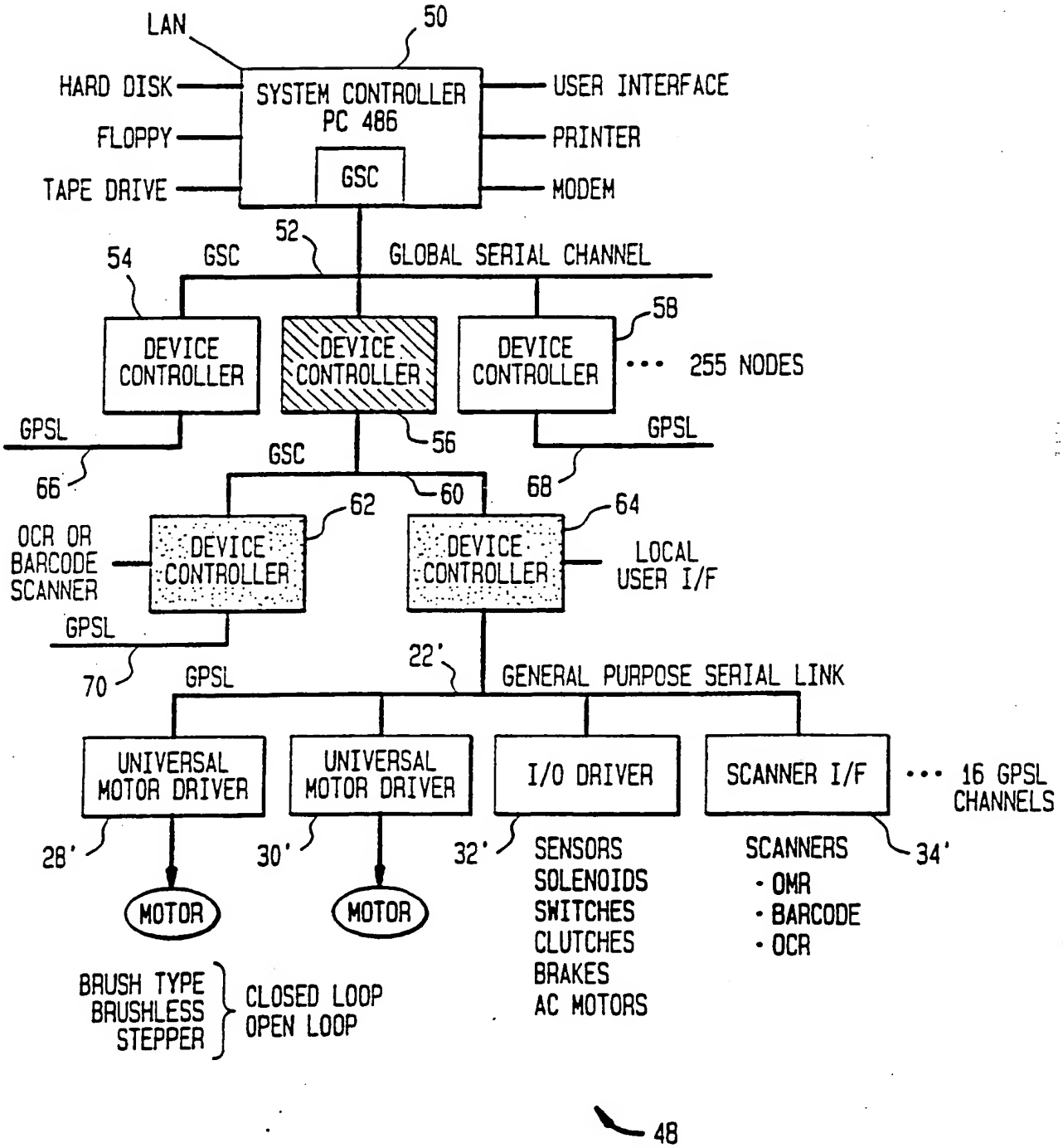

LAN
50
HARD DISK
SYSTEM CONTROLLER
PC 486
USER INTERFACE
FLOPPY
PRINTER
GSC
TAPE DRIVE
MODEM
52
54
GSC
GLOBAL SERIAL CHANNEL
58
DEVICE CONTROLLER
DEVICE CONTROLLER
DEVICE CONTROLLER
255 NODES
GPSL
GPSL
56
GSC
66
60
68
62
64
OCR OR BARCODE SCANNER
DEVICE CONTROLLER
DEVICE CONTROLLER
LOCAL USER I/F
GPSL
22'
70
GPSL
GENERAL PURPOSE SERIAL LINK
UNIVERSAL MOTOR DRIVER
UNIVERSAL MOTOR DRIVER
I/O DRIVER
SCANNER I/F
16 GPSL CHANNELS
28'
30'
32'
34'
SENSORS
SOLENOIDS
SWITCHES
CLUTCHES
BRAKES
AC MOTORS
SCANNERS
• OMR
• BARCODE
• OCR
MOTOR
MOTOR
BRUSH TYPE
BRUSHLESS
STEPPER
CLOSED LOOP
OPEN LOOP
48

FIG. 3

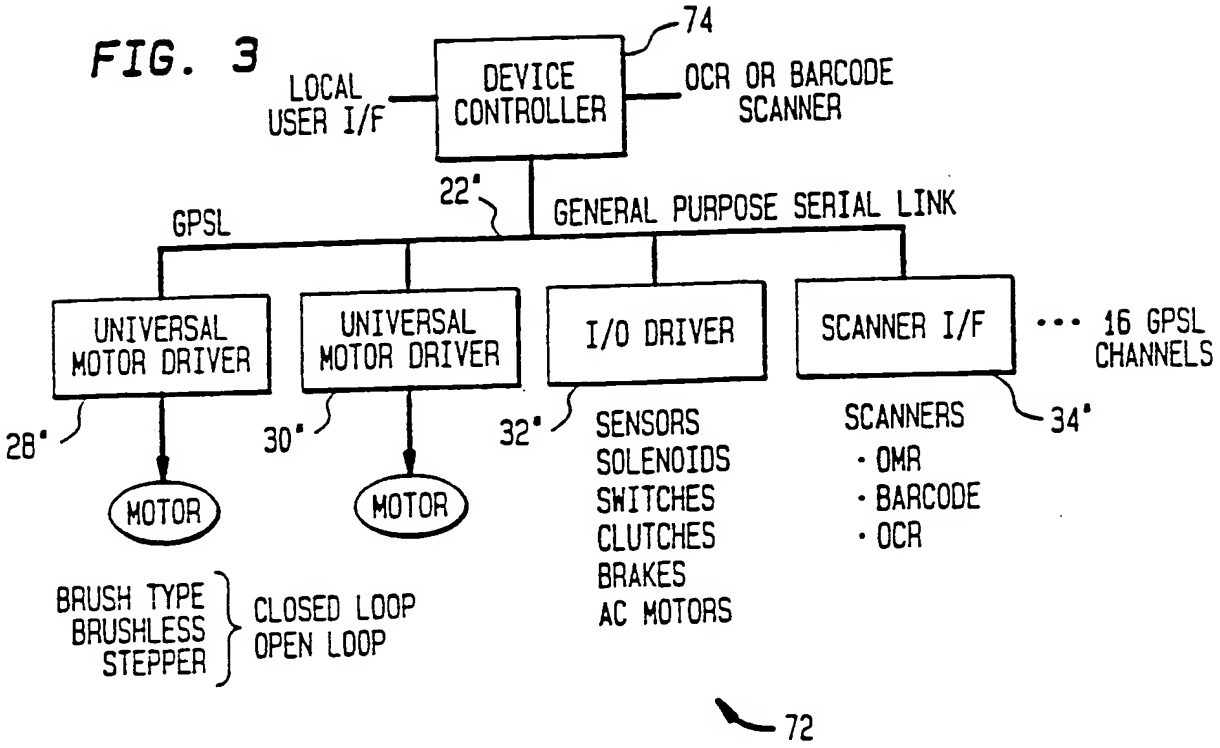

74
LOCAL USER I/F
DEVICE CONTROLLER
OCR OR BARCODE SCANNER
22'
GENERAL PURPOSE SERIAL LINK
GPSL
UNIVERSAL MOTOR DRIVER
UNIVERSAL MOTOR DRIVER
I/O DRIVER
SCANNER I/F
16 GPSL CHANNELS
28'
30'
32'
34'
MOTOR
MOTOR
SENSORS
SOLENOIDS
SWITCHES
CLUTCHES
BRAKES
AC MOTORS
SCANNERS
· OMR
· BARCODE
· OCR
BRUSH TYPE
BRUSHLESS
STEPPER
CLOSED LOOP
OPEN LOOP
72

FIG. 4

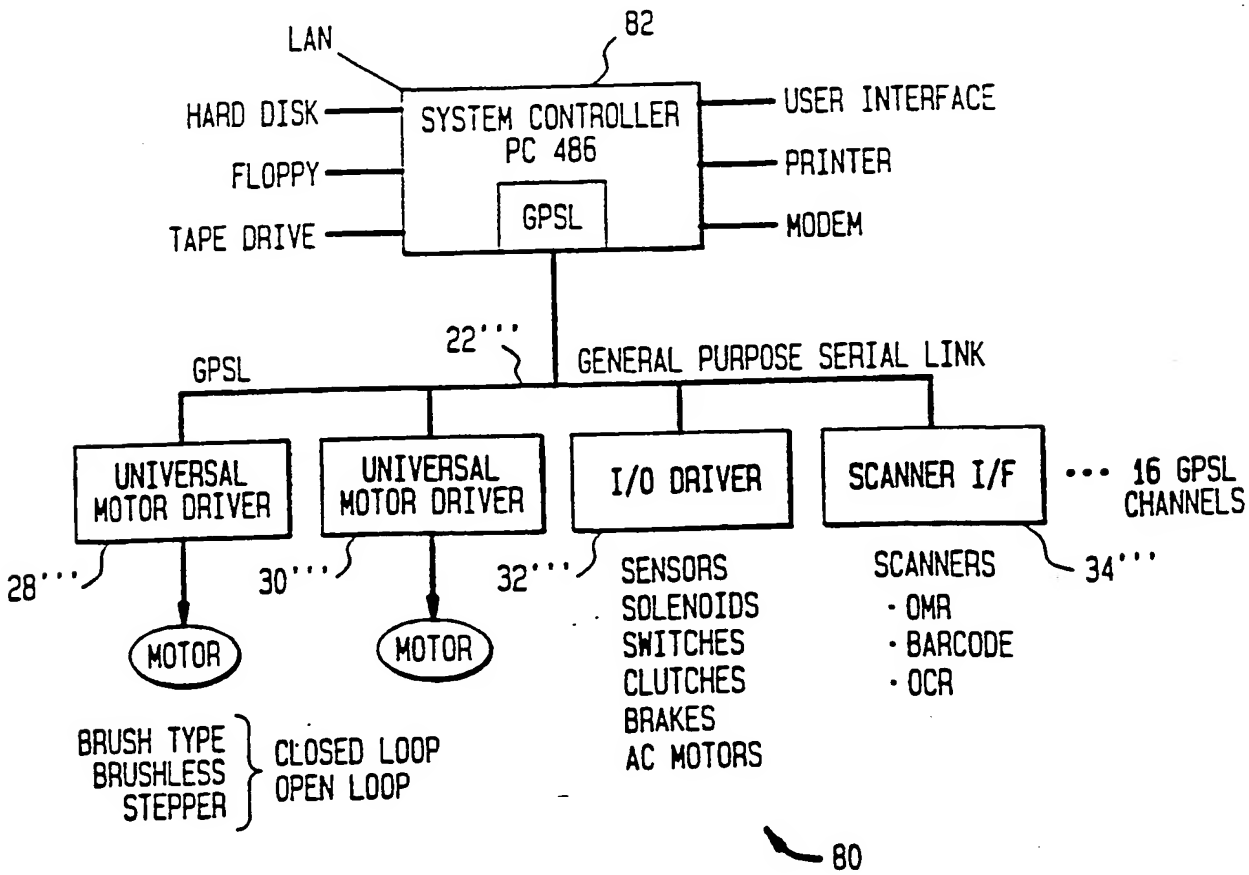

LAN
82
HARD DISK
FLOPPY
TAPE DRIVE
SYSTEM CONTROLLER PC 486
GPSL
USER INTERFACE
PRINTER
MODEM
22'''
GENERAL PURPOSE SERIAL LINK
GPSL
UNIVERSAL MOTOR DRIVER
UNIVERSAL MOTOR DRIVER
I/O DRIVER
SCANNER I/F
16 GPSL CHANNELS
28'''
30'''
32'''
34'''
MOTOR
MOTOR
SENSORS
SOLENOIDS
SWITCHES
CLUTCHES
BRAKES
AC MOTORS
SCANNERS
· OMR
· BARCODE
· OCR
BRUSH TYPE
BRUSHLESS
STEPPER
CLOSED LOOP
OPEN LOOP
80

FIG. 5

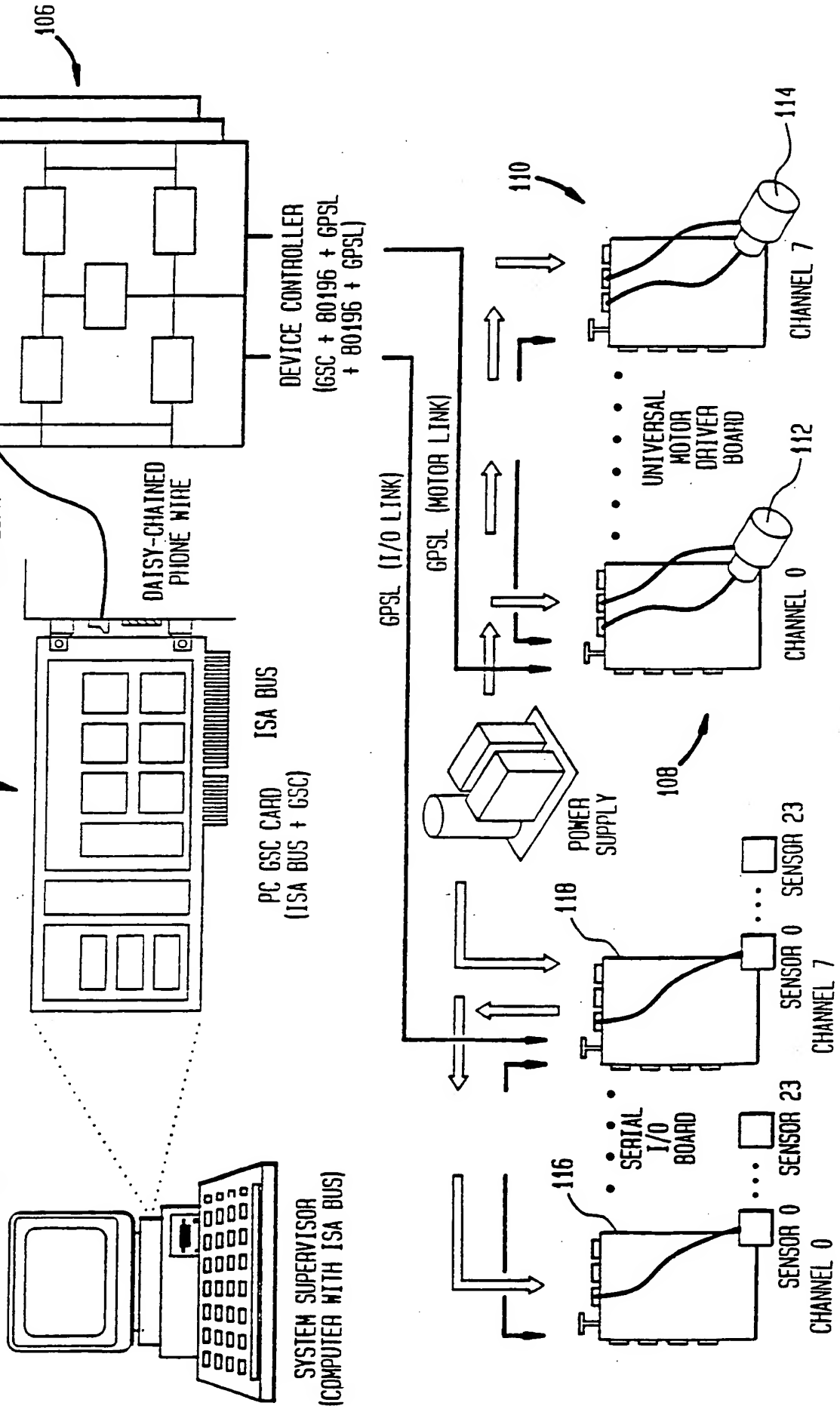

106
DEVICE CONTROLLER
(GSC + 80196 + GPSL
+ 80196 + GPSL)
GSC LINK
DAISY-CHAINED
PHONE WIRE
104
PC GSC CARD
(ISA BUS + GSC)
ISA BUS
102
SYSTEM SUPERVISOR
(COMPUTER WITH ISA BUS)
GPSL (I/O LINK)
GPSL (MOTOR LINK)
110
114
CHANNEL 7
UNIVERSAL
MOTOR
DRIVER
BOARD
112
CHANNEL 0
108
POWER
SUPPLY
118
SENSOR 0
SENSOR 23
CHANNEL 7
SERIAL
I/O
BOARD
116
SENSOR 0
SENSOR 23
CHANNEL 0

FIG. 6

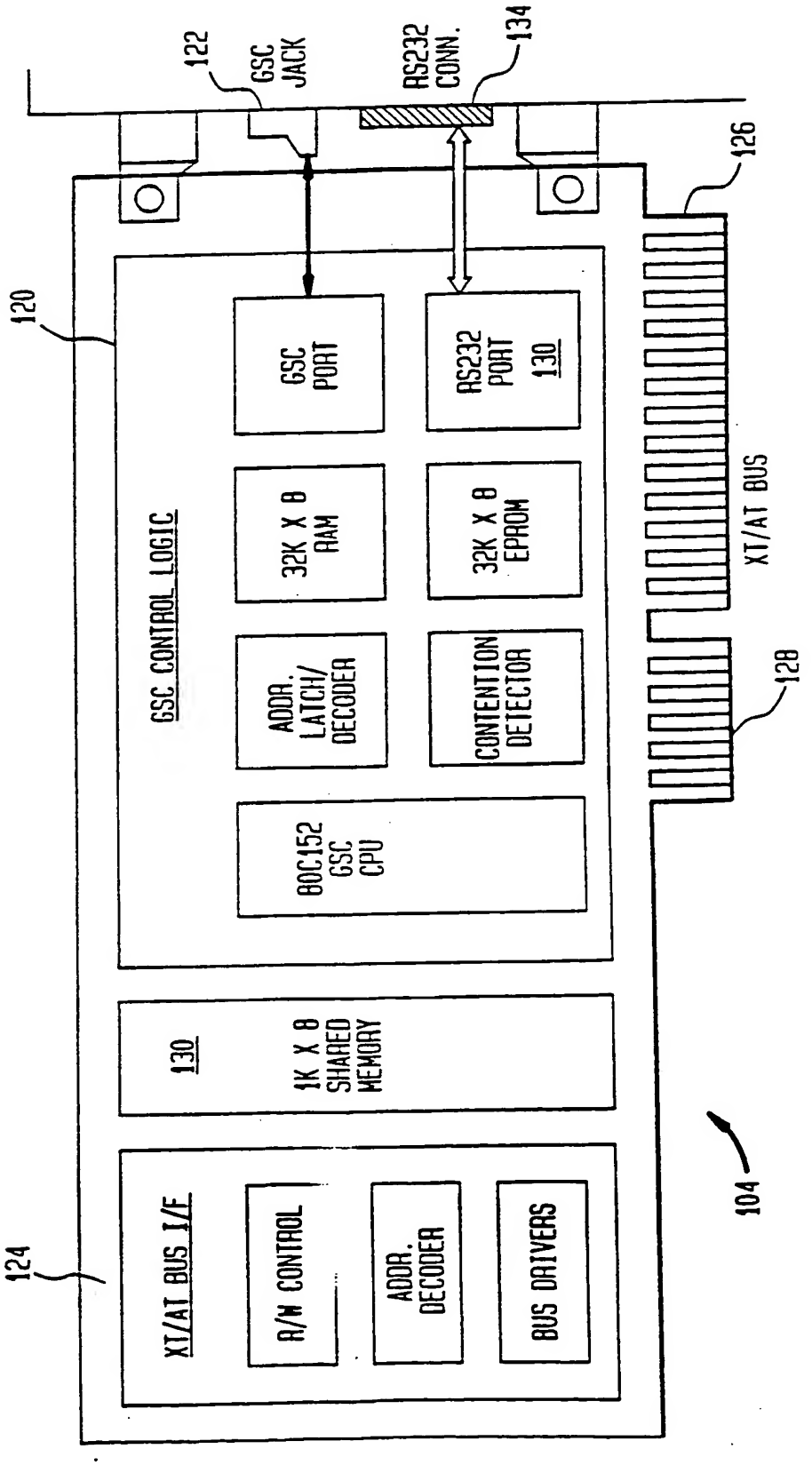

122
GSC JACK
RS232 CONN.
134
126
120
GSC CONTROL LOGIC
GSC PORT
RS232 PORT 130
32K X 8 RAM
32K X 8 EPROM
ADDR. LATCH/ DECODER
CONTENTION DETECTOR
80C152 GSC CPU
XT/AT BUS
128
130
1K X 8 SHARED MEMORY
104
124
XT/AT BUS I/F
R/W CONTROL
ADDR. DECODER
BUS DRIVERS

FIG. 7

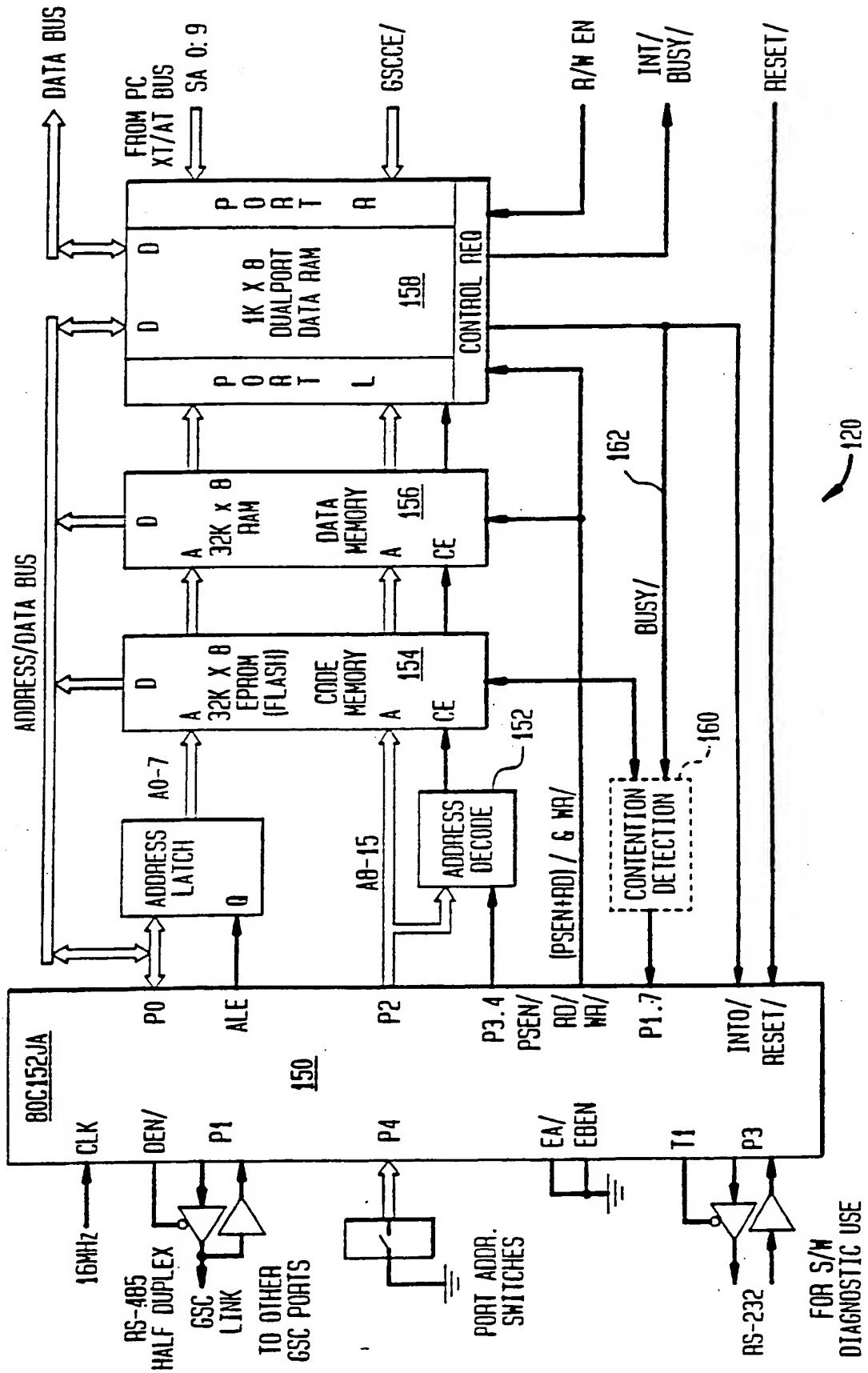

DATA BUS
FROM PC XT/AT BUS
SA 0:9
GSCCE/
R/W EN
INT/ BUSY/
RESET/
1K X 8 DUALPORT DATA RAM
158
CONTROL REG
PORT L
PORT R
32K x 8 RAM
DATA MEMORY
156
32K X 8 EPROM (FLASH)
CODE MEMORY
154
ADDRESS/DATA BUS
A0-7
ADDRESS LATCH
A8-15
ADDRESS DECODE
152
162
BUSY/
CONTENTION DETECTION
160
120
80C152JA
150
CLK
16MHz
OEN/
RS-485 HALF DUPLEX
P1
GSC LINK
TO OTHER GSC PORTS
P4
PORT ADDR. SWITCHES
P0
ALE
P2
P3.4 PSEN/
RD/ WR/
(PSEN+RD) / & WR/
EA/ EBEN
P1.7
T1
INT0/ RESET/
P3
RS-232
FOR S/W DIAGNOSTIC USE

FIG. 8

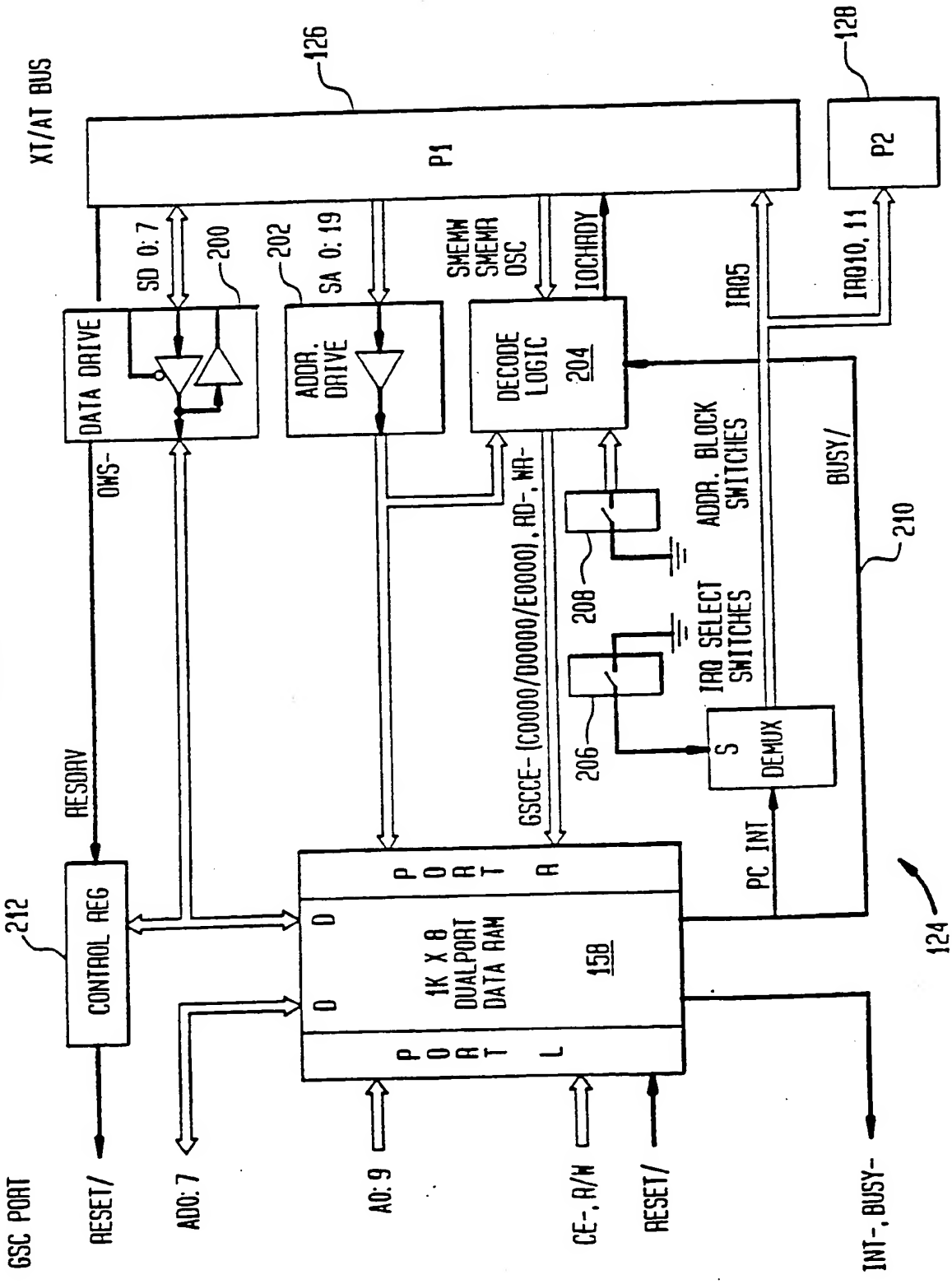

XT/AT BUS
126
P1
128
P2
SD 0:7
200
202
SA 0:19
SMEMW
SMEMR
OSC
IOCHRDY
IRQ5
IRQ10, 11
DATA DRIVE
ADDR. DRIVE
DECODE LOGIC
204
ADDR. BLOCK SWITCHES
IRQ SELECT SWITCHES
208
206
S
DEMUX
PC INT
BUSY/
210
OWS-
RESDRV
GSCCE-(C0000/D0000/E0000), RD-, WR-
212
CONTROL REG
PORT A
D
D
1K X 8 DUALPORT DATA RAM
158
PORT L
124
GSC PORT
RESET/
AD0:7
A0:9
CE-, R/W
RESET/
INT-, BUSY-

FIG. 9

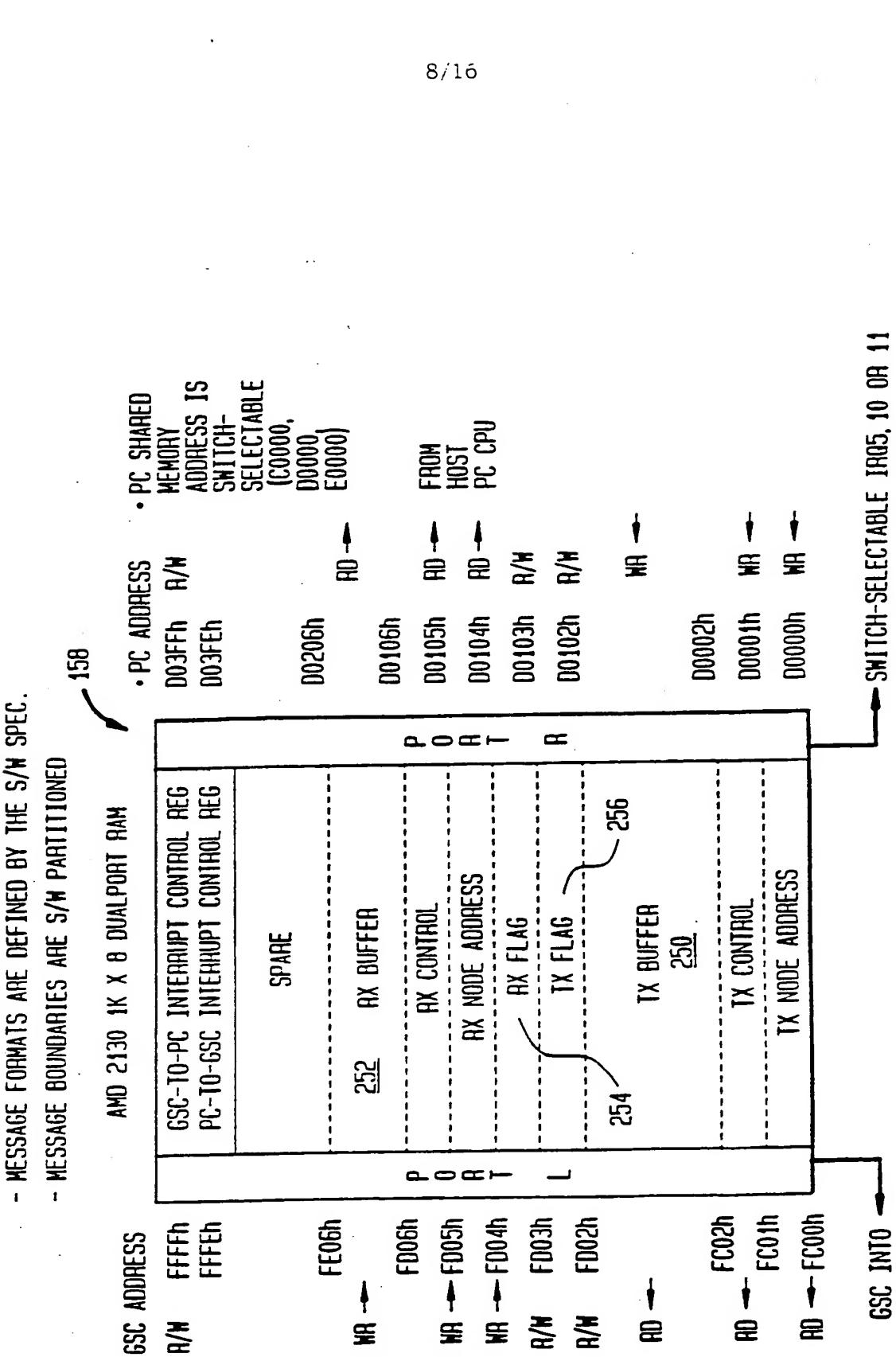

- MESSAGE FORMATS ARE DEFINED BY THE S/W SPEC.
- MESSAGE BOUNDARIES ARE S/W PARTITIONED
158
AMD 2130 1K X 8 DUALPORT RAM
GSC-TO-PC INTERRUPT CONTROL REG
PC-TO-GSC INTERRUPT CONTROL REG
SPARE
252 RX BUFFER
RX CONTROL
RX NODE ADDRESS
RX FLAG
TX FLAG
256
254
TX BUFFER
250
TX CONTROL
TX NODE ADDRESS
PORT L
PORT R
GSC ADDRESS
R/W
FFFFh
FFFEh
FE06h
WR
FD06h
WR
FD05h
WR
FD04h
R/W
FD03h
R/W
FD02h
RD
FC02h
RD
FC01h
RD
FC00h
GSC INTO
FROM 80C152 GSC CPU
• PC ADDRESS
D03FFh R/W
D03FEh
D0206h
RD
D0106h
D0105h
RD
D0104h
RD
D0103h R/W
D0102h R/W
WR
D0002h
D0001h
WR
D0000h
WR
• PC SHARED MEMORY ADDRESS IS SWITCH-SELECTABLE (C0000, D0000, E0000)
FROM HOST PC CPU
SWITCH-SELECTABLE IRQ5, 10 OR 11

FIG. 10

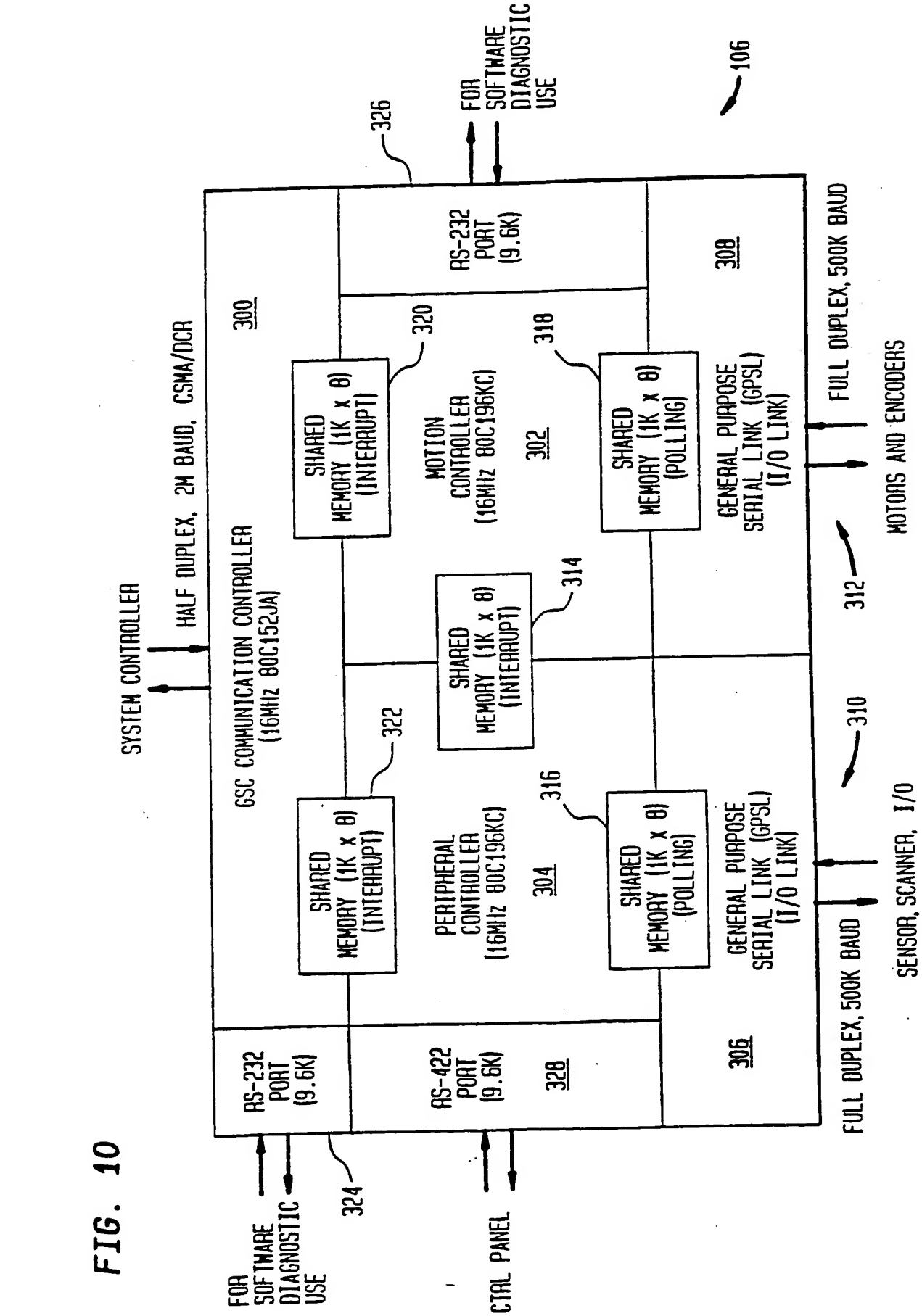
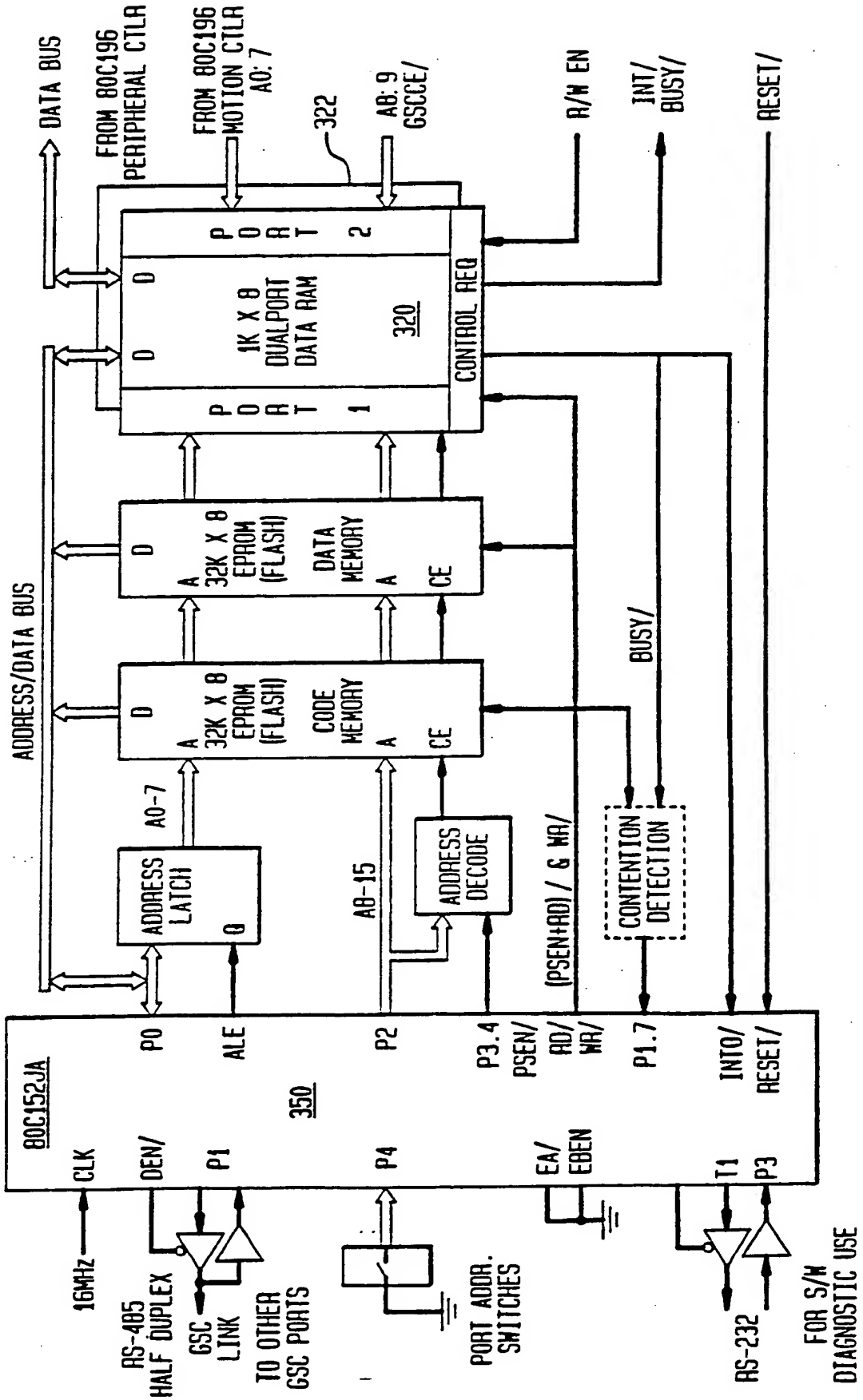

SYSTEM CONTROLLER
HALF DUPLEX, 2M BAUD, CSMA/DCA
GSC COMMUNICATION CONTROLLER (16MHz 80C152JA)
300
SHARED MEMORY (1K x 8) (INTERRUPT)
320
MOTION CONTOLLER (16MHz 80C196KC)
302
318
SHARED MEMORY (1K x 8) (POLLING)
GENERAL PURPOSE SERIAL LINK (GPSL) (I/O LINK)
308
326
RS-232 PORT (9.6K)
FOR SOFTWARE DIAGNOSTIC USE
106
FULL DUPLEX, 500K BAUD
312
MOTORS AND ENCODERS
SHARED MEMORY (1K x 8) (INTERRUPT)
314
322
SHARED MEMORY (1K x 8) (INTERRUPT)
PERIPHERAL CONTOLLER (16MHz 80C196KC)
304
316
SHARED MEMORY (1K x 8) (POLLING)
GENERAL PURPOSE SERIAL LINK (GPSL) (I/O LINK)
306
310
FULL DUPLEX, 500K BAUD
SENSOR, SCANNER, I/O
RS-232 PORT (9.6K)
324
RS-422 PORT (9.6K)
328
FOR SOFTWARE DIAGNOSTIC USE
CTRL PANEL

FIG. 11


DATA BUS
FROM 80C196 PERIPHERAL CTLR
FROM 80C196 MOTION CTLR
A0:7
322
AB:9
GSCCE/
R/W EN
INT/ BUSY/
RESET/
1K X 8 DUALPORT DATA RAM
320
PORT 2
PORT 1
CONTROL REQ
32K X 8 EPROM (FLASH) DATA MEMORY
32K X 8 EPROM (FLASH) CODE MEMORY
ADDRESS/DATA BUS
ADDRESS LATCH
A0-7
AB-15
ADDRESS DECODE
(PSEN+RD) / & WR/
BUSY/
CONTENTION DETECTION
80C152JA
350
CLK
DEN/
P1
P4
EA/ EBEN
T1
P3
P0
ALE
P2
P3.4 PSEN/ RD/ WR/
P1.7
INT0/ RESET/
16MHz
RS-485 HALF DUPLEX
GSC LINK
TO OTHER GSC PORTS
PORT ADDR. SWITCHES
RS-232
FOR S/W DIAGNOSTIC USE

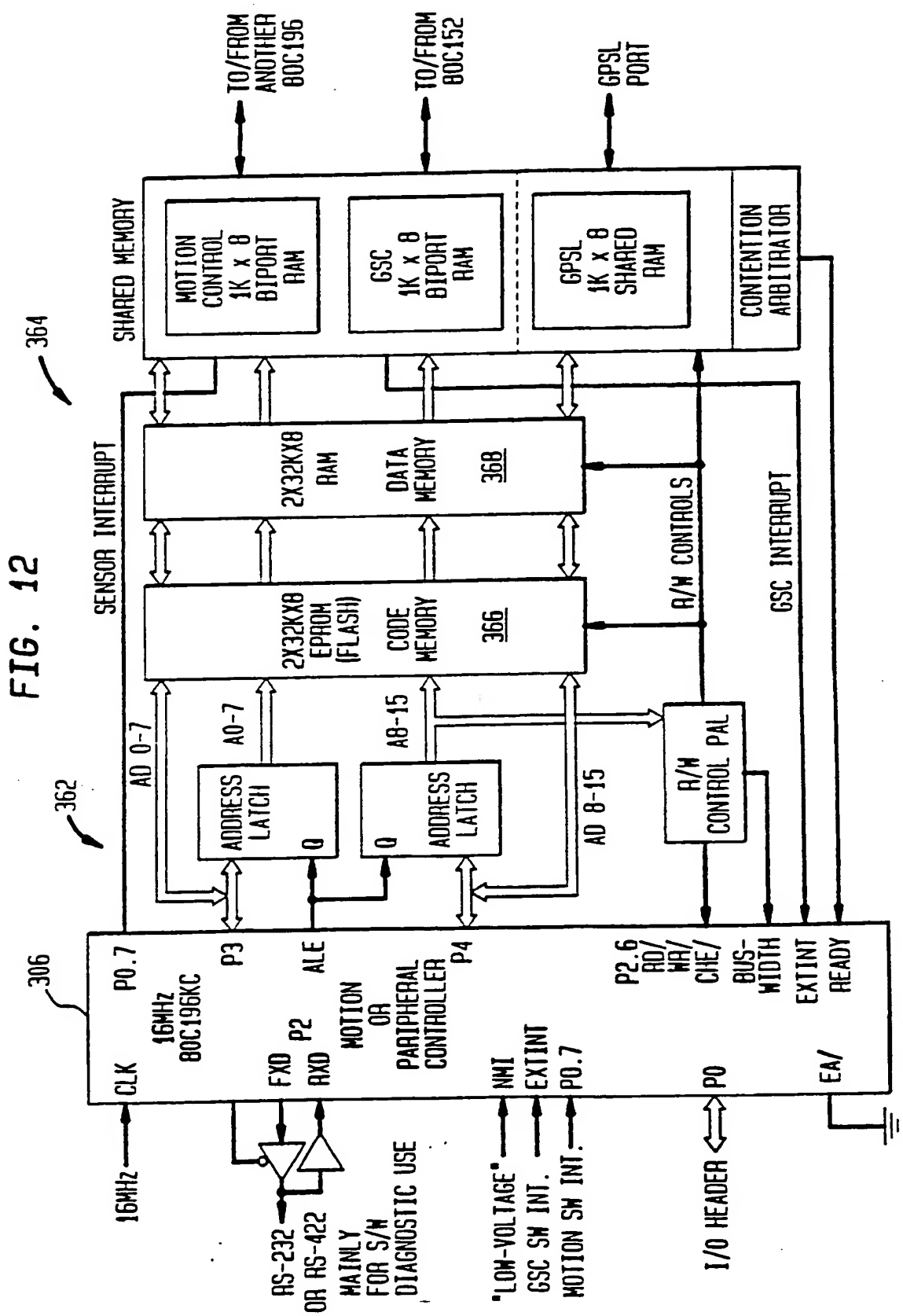

TO/FROM ANOTHER 80C196
TO/FROM 80C152
GPSL PORT
SHARED MEMORY
MOTION CONTROL 1K x 8 DIPORT RAM
GSC 1K x 8 DIPORT RAM
GPSL 1K x 8 SHARED RAM
CONTENTION ARBITRATOR
364
SENSOR INTERRUPT
2X32KX8 RAM
DATA MEMORY
368
2X32KX8 EPROM (FLASH)
CODE MEMORY
366
A/W CONTROLS
GSC INTERRUPT
AD 0-7
A0-7
A8-15
AD 8-15
ADDRESS LATCH
ADDRESS LATCH
A/W CONTROL PAL
362
306
16MHz 80C196KC
CLK
P0.7
P3
ALE
P4
P2
FXD
RXD
MOTION OR PARIPHERAL CONTROLLER
NMI
EXTINT
P0.7
P0
P2.6 RD/ WR/ CHE/
BUS-WIDTH
EXTINT
READY
EA/
16MHz
RS-232 OR RS-422
MAINLY FOR S/W DIAGNOSTIC USE
"LOW-VOLTAGE"
GSC SW INT.
MOTION SW INT.
I/O HEADER

FIG. 12

FIG. 13

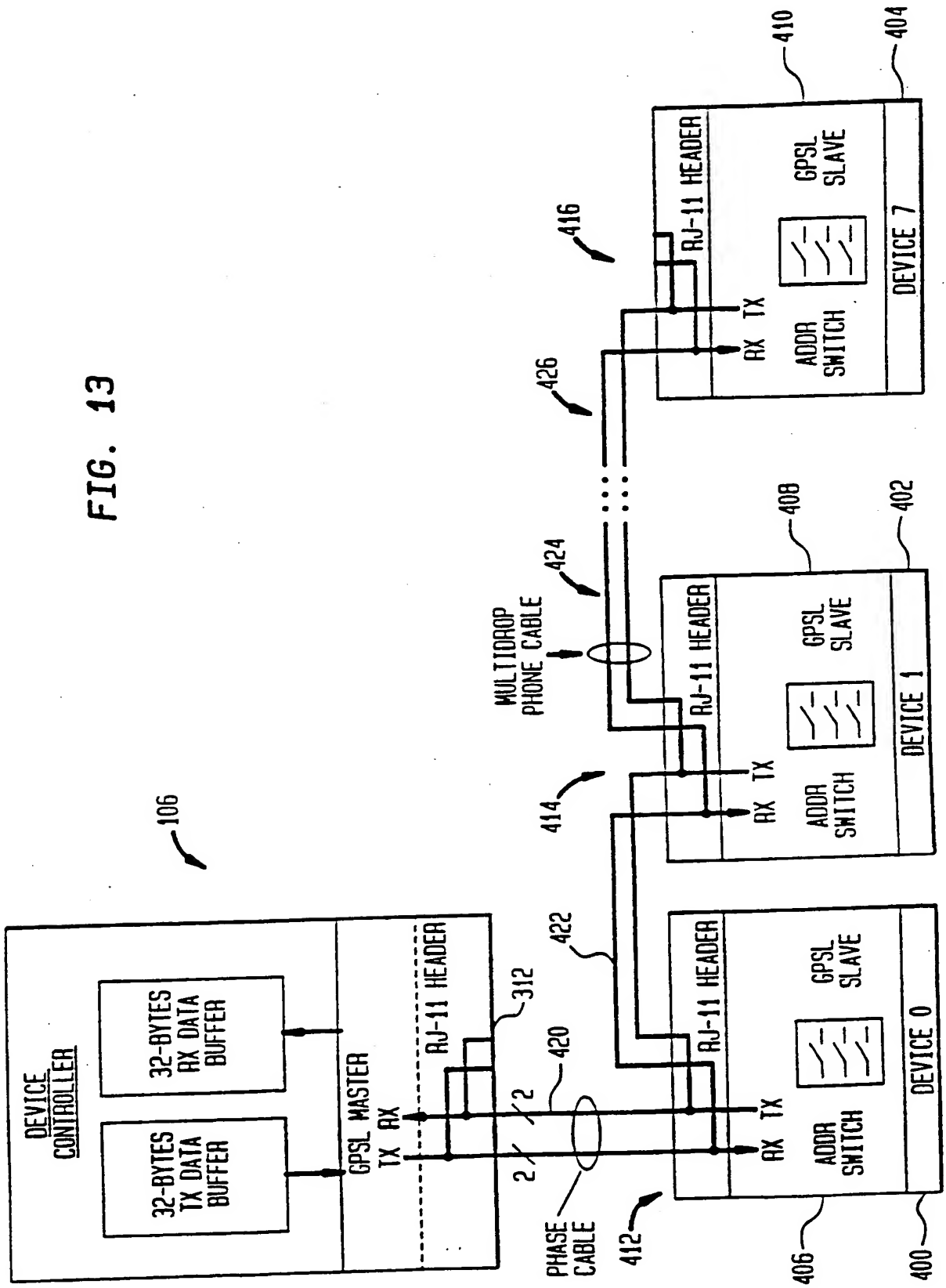

106
DEVICE CONTROLLER
32-BYTES TX DATA BUFFER
32-BYTES RX DATA BUFFER
GPSL MASTER
TX RX
RJ-11 HEADER
312
420
2
2
PHASE CABLE
412
422
414
MULTIDROP PHONE CABLE
424
426
416
RJ-11 HEADER
RX TX
ADDR SWITCH
GPSL SLAVE
DEVICE 0
406
400
408
DEVICE 1
402
410
DEVICE 7
404

FIG. 14

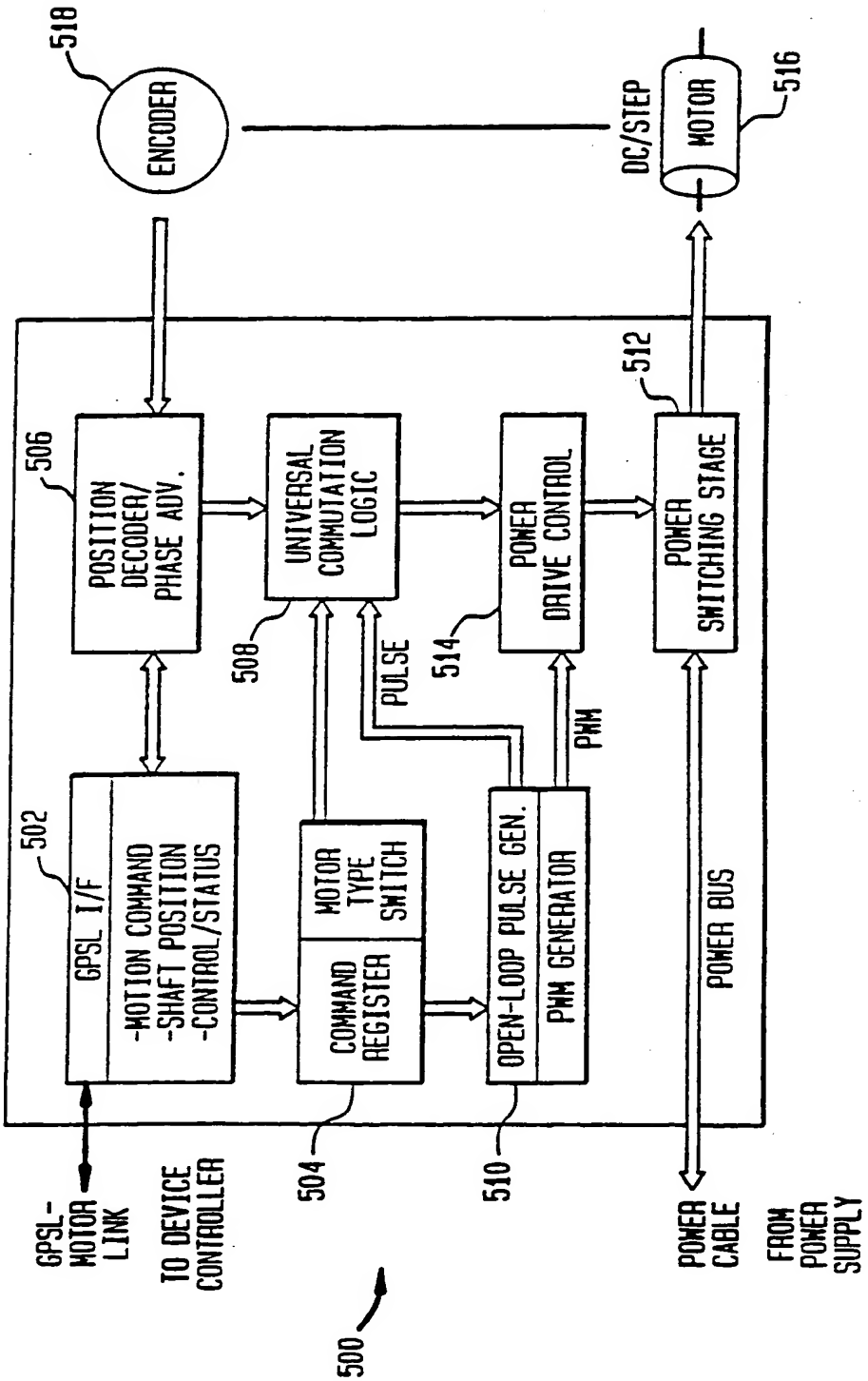

518
ENCODER
DC/STEP
MOTOR
516
506
POSITION DECODER/ PHASE ADV.
UNIVERSAL COMMUTATION LOGIC
POWER DRIVE CONTROL
512
POWER SWITCHING STAGE
508
PULSE
514
PWM
502
GPSL I/F
-MOTION COMMAND
-SHAFT POSITION
-CONTROL/STATUS
MOTOR TYPE SWITCH
COMMAND REGISTER
OPEN-LOOP PULSE GEN.
PWM GENERATOR
POWER BUS
GPSL-MOTOR LINK
TO DEVICE CONTROLLER
504
510
POWER CABLE
FROM POWER SUPPLY
500

FIG. 15

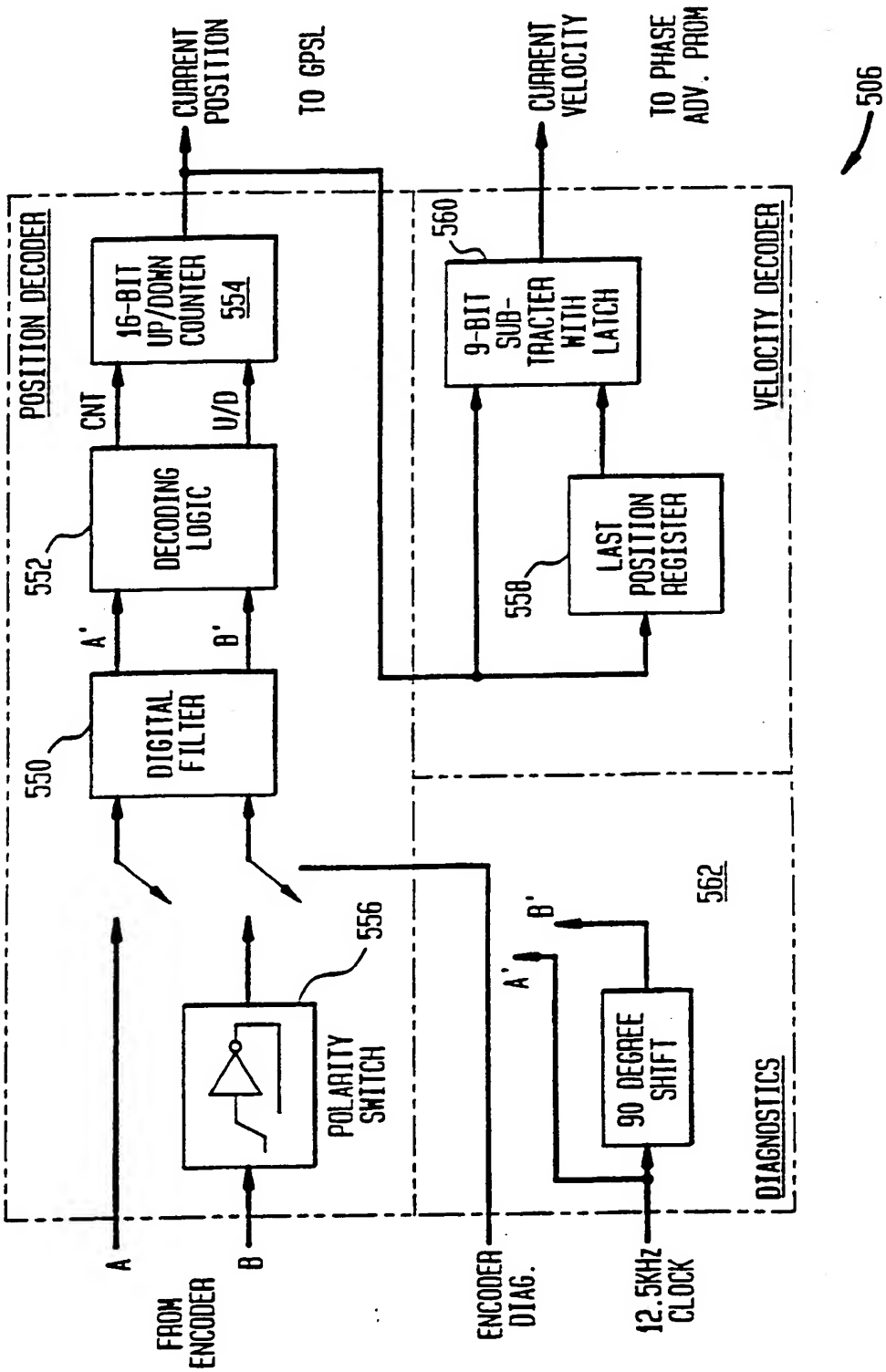

506
POSITION DECODER
VELOCITY DECODER
DIAGNOSTICS
CURRENT POSITION
TO GPSL
CURRENT VELOCITY
TO PHASE ADV. PROM
16-BIT UP/DOWN COUNTER 554
DECODING LOGIC
552
CNT
U/D
A'
B'
DIGITAL FILTER
550
9-BIT SUB-TRACTER WITH LATCH
560
LAST POSITION REGISTER
558
POLARITY SWITCH
556
90 DEGREE SHIFT
562
A
B
FROM ENCODER
ENCODER DIAG.
12.5KHz CLOCK

FIG. 16

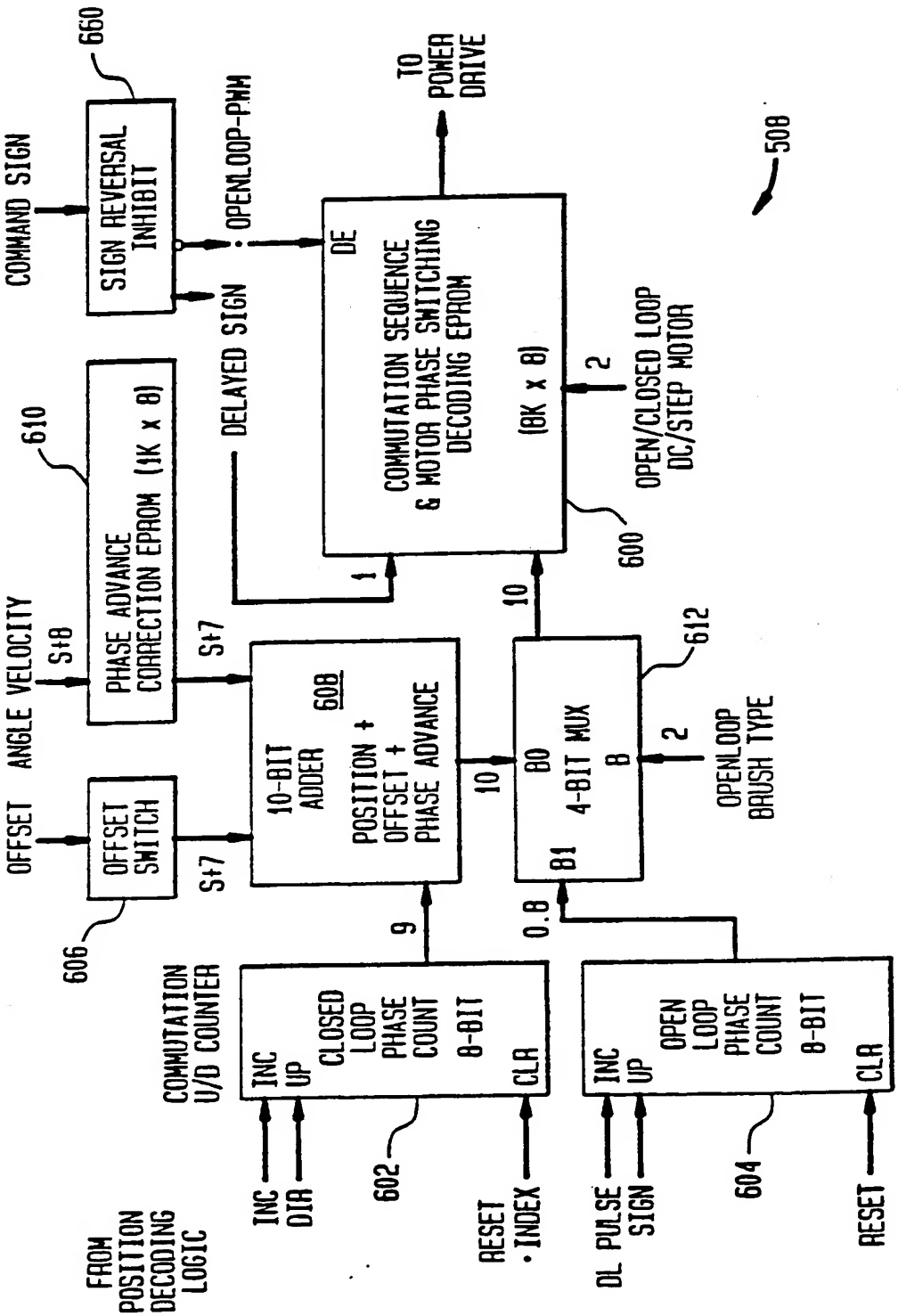
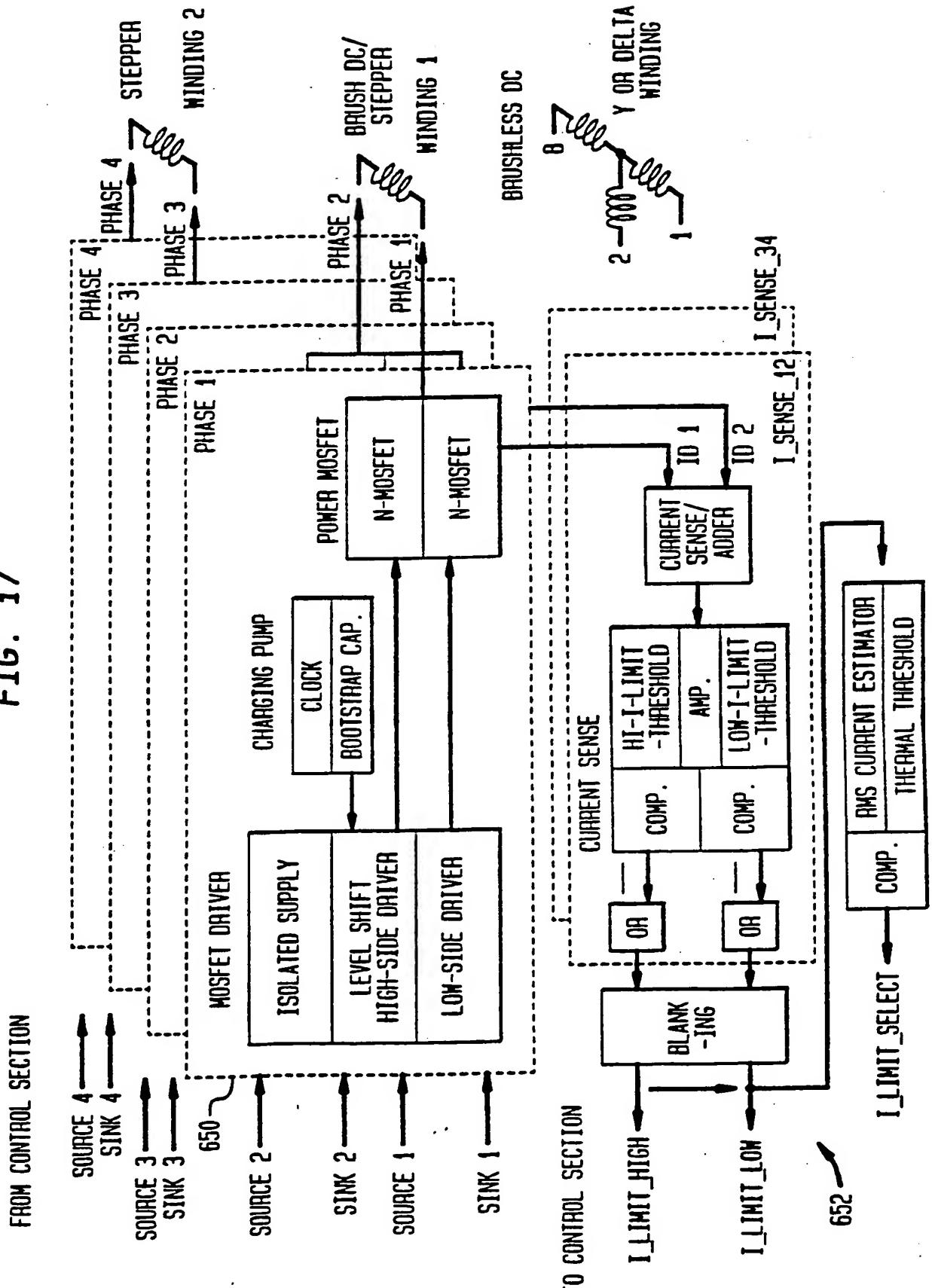

508
660
SIGN REVERSAL INHIBIT
COMMAND SIGN
OPENLOOP-PWM
DELAYED SIGN
TO POWER DRIVE
DE
COMMUTATION SEQUENCE & MOTOR PHASE SWITCHING DECODING EPROM
(8K x 8)
600
OPEN/CLOSED LOOP DC/STEP MOTOR
610
PHASE ADVANCE CORRECTION EPROM (1K x 8)
ANGLE VELOCITY
S+8
S+7
10-BIT ADDER
608
POSITION + OFFSET + PHASE ADVANCE
612
4-BIT MUX
B
OPENLOOP BRUSH TYPE
OFFSET
OFFSET SWITCH
606
COMMUTATION U/D COUNTER
FROM POSITION DECODING LOGIC
INC
DIR
CLOSED LOOP PHASE COUNT 8-BIT
INC
UP
CLR
602
RESET
INDEX
OPEN LOOP PHASE COUNT 8-BIT
DL PULSE
SIGN
604
RESET

FIG. 17


FROM CONTROL SECTION
SOURCE 4
SINK 4
SOURCE 3
SINK 3
650
SOURCE 2
SINK 2
SOURCE 1
SINK 1
MOSFET DRIVER
ISOLATED SUPPLY
LEVEL SHIFT HIGH-SIDE DRIVER
LOW-SIDE DRIVER
CHARGING PUMP
CLOCK
BOOTSTRAP CAP.
POWER MOSFET
N-MOSFET
N-MOSFET
PHASE 4
PHASE 3
PHASE 2
PHASE 1
STEPPER WINDING 2
BRUSH DC/ STEPPER WINDING 1
BRUSHLESS DC
8
2
1
Y OR DELTA WINDING
I_SENSE_34
I_SENSE_12
ID 1
ID 2
CURRENT SENSE/ ADDER
CURRENT SENSE
HI-I-LIMIT -THRESHOLD
AMP.
LOW-I-LIMIT -THRESHOLD
COMP.
COMP.
OR
OR
BLANK -ING
TO CONTROL SECTION
I_LIMIT_HIGH
I_LIMIT_LOW
652
RMS CURRENT ESTIMATOR
THERMAL THRESHOLD
COMP.
I_LIMIT_SELECT

2283836

UNIVERSAL ELECTRICAL SYSTEM ARCHITECTURE FOR CONTROL APPLICATIONS

The invention relates to system architectures for control applications and more particularly to a communication architecture and protocol which can be easily optimized for control of the operation of various desired functions.

Production Mailing apparatus typically has been one of the mail handling devices least susceptible to standardization because of the disparate nature of each customer's applications and the range of volumes of mail to be handled by each different customer. Each mailing apparatus has in the past had to be customized in order to meet the customer's needs. For the manufacturer this has required both expensive re-engineering efforts and an increase in inventory because of the necessity for a large variation in spare electronic boards and other components in order to assure satisfactory customer relations and relatively quick repairs.

It is known to modularize the stations for a stand-alone system as taught, for example, in U.S.Patent 4,547,856 to Piotroski. While this has worked well, the electronic architecture is limited and accommodates only the specific operations of the large production mailing machines and does not easily allow networking with local area networks (LAN's) and other inputs and outputs of present day devices.

U.S. Patent 4,514,799 to Spencer et al. describes a bus system architecture for a microprocessor system

comprising an array of bus lines for communication between and among microprocessors.

U.S. Patent 4,517,637 to Cassell discloses a host system connected to devices via a local area network for operation of the various measurement and control functions. The operation program is centralized and communication with the devices occurs directly through an LAN.

U.S. Patent 4,780,814 describes a global serial channel for a microcontroller while 4,782,439 describes an arrangement utilizing direct memory access (DMA).

None of these references teaches apparatus which may in one universal system architecture be versatile and flexible enough to be used any many different arrangements for controlling many different processes, and which is particularly useful for controlling apparatus used in production mailing devices.

It is therefore an aim of the invention to provide a system architecture particularly useful for production mail apparatus which will, with a minimum number of electronic boards, allow configuring to meet a large range of the various customer requirements.

Thus there is provided in accordance with the invention a system electronic architecture comprising control means for controlling a plurality of determined devices chosen from the group consisting of stepper motors, DC motors and brushless DC motors, said control means communicating with at least one motor drive controller by means of a master-slave communication means, said motor drive controller being operative for controlling at least a selected one of said plurality of devices, said master-slave communication means being a serial communication means, said control means including means for receiving and storing control parameters for operation of said plurality of devices, and said means for receiving including a second

communication means adapted for communication with a system control means.

In a preferred embodiment of the invention, the second communication means is a Global Serial Channel (GSC) communication means.

The invention will be better understood from the following non-limiting description of an example thereof given with reference to the accompanying drawings in which:-

Figure 1 is a block diagram of an example of a control architecture for a communication apparatus in accordance with the invention showing Peer-to-Peer relationships;

Figure 2 is a block diagram of another example of a control architecture in accordance with the invention showing additional Master-Slave relationships along with the Peer-to-Peer relationships;

Figure 3 is a block diagram showing a single-layer architecture using a device controller in a communication apparatus in accordance with the invention;

Figure 4 is a block diagram of a single-level architecture using a system controller in a communication apparatus in accordance with the invention;

Figure 5 is a system configuration for use with an inserter using the four "building block" boards as may be employed in accordance with the invention;

Fig. 6 is a view of a Global Serial Channel board for use with an off-the-shelf PC.

Fig. 7 is a block diagram of the GSC port on the GSC board.

Fig. 8 is a block diagram of an XT/AT bus interface on the GSC board.

Fig. 9 is shows a suitable memory map for the shared memory of the GSC board.

Fig. 10 is a block diagram of the device control board.

Fig. 11 is a block diagram of the GSC communication interface of the device control board.

Fig. 12 is a block diagram of the motion/peripheral control processor of the device control board.

Fig. 13 is a block diagram of the GPSL communication link.

Fig. 14 is a block diagram of a universal drive board usable in the invention;

Fig. 15 is a block diagram of the decoder circuit of the universal drive board.

Fig. 16 is a block diagram of the universal commutation logic circuit.

Fig. 17 is block diagram of the power switching circuitry of the universal drive board.

In Fig. 1, there is shown generally at 10 a system in accordance with the invention showing peer-to-peer relationships. The architecture of the system comprises an modular arrangement which is expandable and flexible and which is configurable with either centralized or distributed processing. This flexibility makes it applicable to a wide variety of system control applications for a range from small to very large systems.

The system architecture is shown in Fig. 1 generally at 10. As seen in this Figure, the system controller 12 is the backbone of the Global Serial Channel (GSC) network shown at 14 for the illustrated distributed multi-layer control applications. It will be understood that for smaller applications it may be configured as a centralized controller with direct access to the General Purpose Serial Link as seen below in connection with Fig. 4. The system controller 12 interfaces in conventional manner to external local area networks (LAN'S), storage media such as hard disks, floppy disks, tape drives, and the like, printers, modems, or large scale user interfaces as desired.

A plurality of Device Controllers illustrated at 16, 18 and 20, respectively, communicate on the GSC network and as required on the General Purpose Serial Link (GPSL) 22 which will be described below. The GSC is preferably an

Intel bus arrangement as described in U.S. Pat. 4,780,814 to Hayak and marketed by Intel as the 80C152 Universal Communication Controller Chip. The device will support up to 255 device controllers only three of which are shown here.

Controller 16 is shown interfacing to the local user at port 24 and to an OCR or Barcode scanner at 26. Universal Motor Drivers 28 and 30 as well as I/O Driver 32 and Scanner I/F 34 communicate with Device Controller 18 via the GPSL 22. In a preferred embodiment, the General Purpose Serial Link 22 in accordance with the invention will be able to accommodate 16 channels of information. The GPSL channels as illustrated may be configured for motion control communication with the Motor Drivers, for I/O control or for scanner control.

The motor drivers, two of which are shown in Fig. 1 for illustrative purposes can provide both closed and open loop motion control for DC brush type motors, DC brushless motors, and DC stepper motors as desired. These drivers will be discussed further below.

The I/O Driver 32 provides control for up to 16 inputs and up to 8 outputs. The I/O as controls sensors, solenoids, clutches, brakes, actuators, and/or AC motors.

The scanner interface 34 decodes and interprets OMR scan marks and barcodes. It may also serve as an interface to serial OCR and Barcode scanners.

Figs. 2, 3, and 4 illustrate the flexibility of the system architecture in accordance with the invention. Fig. 2 shows a multi-layer distributed architecture utilizing both peer-to-peer and master-slave relationships. In this arrangement, the system controller 50 communicates along Global Serial Channel 52 with device controllers 54, 56, and 58, respectively. In this configuration, device controller 56 communicates on a GSC with two additional device controllers 62 and 64 in a master-slave relationship. For example the device controller 64 may control a local user interface in addition to controlling the motors and I/O and scanner interface as previously describe in Fig. 1. The

parts here are labelled with primes in order to show the similarity of this layer of control. Device controllers 54 and 58 may communicate with additional devices via GPSL 66 and 68, respectively. The other device controller 62 which operates in this configuration as a slave to the master device controller 56 may, for example, interface with an OCR or Barcode scanner and communicate with other elements via the GPSL indicated at 70.

Fig. 3 illustrates an example of a single-layer centralized architecture using a device controller configured as a central controller for control of the system and is especially applicable to those systems not requiring access to external LAN's or storage media. In the example of Fig. 3, the device controller 74 interfaces with OCR or Barcode scanners using serial communication and also interfaces with the user with a "low scale" interface. Communications with the motors and other interfaces and scanners are as previously described and again the relationship is recalled by the use of double primes for the features similar to those of Fig. 1.

Fig. 4 shows an example of single layer centralized architecture using the system controller for control. In this example the system controller 82 communicates with the motors and I/O driver and scanner interface via the GPSL without intermediate device controllers. Again to illustrate the similarity, the devices and communication link are labelled with numbers bearing triple primes in correspondence with those described in connection with Fig. 1. The controller 82 provides high-level functions where access to external LAN's or storage media is required.

Fig. 5 shows generally at 100 a suitable embodiment of a control system in accordance with the invention in schematic form for an inserter. The system is suitably configured with a modular design. In accordance with the invention, four different types of boards provide the building blocks. They are the system supervisor shown at 102 which includes the Global Serial Channel communication board 104 to oversee the overall system control. The next

type of block is the device control board shown at 106 to perform the local control of motors and other I/O devices for each mechanical module. Another type of board, the universal motor drive illustrated at two places, 108 and 110, in the Fig. may be configured to drive a variety of motors illustrated here at 112 and 114, respectively. Serial I/O boards shown at 116 and 118 are used to interface with sensors and other I/O devices.

It will be appreciated that almost any motion control application can be implemented by use of determined combinations of these boards. A significant advantage of the use of these modules is that the architecture will shorten product development time and will reduce the cost of inventory which must be carried.

Fig. 6 shows the GSC board configured as a card for insertion into an expansion slot of a typical personal computer (PC) such as the one illustrated at 102 of Fig. 5. The GSC card can provide a GSC communication bus in an ISA bus personal computer. Such a card links the system controller, shown here as the PC 102, with the device controller 106 of Fig. 5. The card consists of three functional blocks described more completely below. The first is a GSC Control Logic section 120 which preferably utilizes an 80C152 GSC CPU available from Intel for communication with device controllers through a GSC cable via jack 122. The second functional block is preferably an ISA bus interface block indicated generally at 124 to communicate with the PC's CPU via the on-board ISA edge connectors 126 and 128. The third functional block is a shared memory 130 to serve as message buffer between the two blocks.

It will be understood that the GSC communication may be made with other system control devices replacing the personal computer and other types of bus arrangements may be implemented for inputting information to the shared memory in place of the illustrated XT/AT bus. An RS232 port 132 is in communication with RS232 connector 134. The port enables

diagnostic communication with the Intel 80C152 device and will not be further described here.

Fig. 7 is a block diagram of the GSC control logic section 120. The GSC control logic section establishes a communication protocol among the System supervisor and the device controllers. The Universal Communication Controller 150, suitably the Intel 80C152 mentioned previously, provides a multi-protocol, 2M baud GSC serial communication which is optimized to implement CSMA/DCR protocol well known in the art. The 80C152 device is capable of supporting up to 32 GSC nodes. The physical connections may suitably be implemented by a full duplex RS-485 multipoint bus transmission. A telephone cable is conveniently used to carry these two differential data signals which swing between 0V and +5V. A modular phone jack is used as the connector receptacle.

Address decode logic 152 demultiplexes in conventional manner the CPU address from the address/data bus. The decoder 152 also decodes the address to enable the appropriate memory for accessing. Eprom 154, suitably 32K bytes, provides code storage. There is also suitably a 32K bytes SRAM 156 for data storage and 1K bytes dual port SRAM 158 to serve as the message buffer.

It will be appreciated that the PC's CPU and the CPU 150 are exchanging information through the dual port memory 158. If both CPU's are writing to the same memory location at the same time the data may be garbled. Therefore, when a contention is detected at the memory 158, the internal arbitration logic in the dualport memory will grant priority to one of the two CPU's, and the other will receive a busy signal. The 80C152 does not have a built-in capability to lengthen memory cycle. Contention Detection circuit 160 will hold the busy signal (received on line 162) on one of the the 80C152's I/O lines so that the 80C152 will keep repeating the previous memory cycle until such time as the function is completed.

Turning now to the PC bus, Fig. 8 shows the XT/AT bus interface block diagram at 124. This block has three major

components. Drivers 200 and 202 serve in known manner to control the data flow and to enhance the driving capability of the Data/Address bus of the PC. The read/write control logic block 204 decodes ISA bus control signals to provide chip-enable signals to memory and peripheral devices and to enable the personal computer to read and write to the shared memory 158. Preferably, the ISA IRQ lines and starting address of the shared memory are selectable via switches 206 and 208, respectively. The busy signal is fed on line 210 from the RAM 158 to the decode logic block 204. Control register 212 is suitably a write-only control register which may be used to hold bits for resetting the 80C152 and for a NO-WAIT-STATE ENABLE for the XT/AT bus.

Fig. 9 is a preferred embodiment of a memory map of the shared memory 158. This memory block provides 1,024 byte message buffers for information exchange between the personal computer and the GSC controller. In the arrangement in accordance with the invention, the shared memory 158 is divided into a transmission buffer area 250 and a receiving buffer area 252, and the information exchange is preferably accomplished by a so-called "mailbox" scheme. The GSC controller 150 (Fig. 7) writes a message to the receiving buffer in the receiving buffer area 252 and sets a flag in a special location such as buffer 254 to interrupt the personal computer via the ISA bus. Then the personal computer reads the message from the receiving buffer and acknowledges the interrupt by resetting the flag in buffer 254. Conversely, the personal computer writes a message into a transmission buffer location in the transmission buffer area 250 and sets a flag in another special memory location such as buffer 256 to interrupt the GSC controller. The GSC controller reads data from the transmission buffer and acknowledges the interrupt by resetting the flag in buffer 256.

For convenience the addresses of the PC shared memory are switch selectable by use, for example, of switch 208 (Fig. 8).

Fig. 10 is a block diagram of a device control board in accordance with the invention. The device control board indicated generally at 106 in correspondence with the board illustrated in Fig. 5 comprises five major functional blocks. As illustrated, there is a GSC communication interface 300 to communicate with the system controller and with other device controllers not shown here via GSC cable. The GSC communication interface utilizes the Intel 80C152 as described previously in respect of the GSC board and will not be further described here.

Motion Controller 302 preferably comprises an Intel 80C196 based Motion Control Processor to generate motion profiles and to control up to eight motor drivers which may be either open-loop or closed-loop controlled devices not shown in this Figure.

Peripheral controller 304 is preferably an Intel 80C196 microprocessor which can interface to up to 128-input lines and up to 128-output lines. It will be understood that each input can be connected to receive input signals from photocells, switches and the like while the output lines may connect to devices such as solenoids, indicators, and the like all of which are not shown in the Figure. The general purpose Serial Link sections (GPSL) 306 and will be discussed below. In general terms, it comprises full duplex, 500K Baud communication links as indicated at 310 and 312 for communication with up to eight universal motor driver boards (not shown) or eight serial I/O boards (not shown) via a serial cable (not shown). The data is formatted in cyclical frames.

Shared memories 314, 316, 318, 320, and 322 are preferably used as message buffers among the processors in the various sections. Other means for communicating between and among the sections will occur to those skilled in the art and may be substituted for the shared memories if desired. The shared memories 316 and 318 are divided into two areas, a transmission buffer and a receiving buffer with the exchange done via a mailbox scheme as described above for the GSC communication. These memory buffers preferably

comprise one transmit buffer and two receive buffers, each buffer having 32 bytes. One receive buffer is arranged to receive all odd number frames and the other is arranged to receive all even number frames of data. Instead of an interrupt, the GPSL controller uses a polling scheme for scanning the receive buffers and writes to the transmit buffer periodically.

In accordance with the mailbox scheme in respect of the other exchanges of data, one processor writes a message into the receiving buffer, and sets a flag in a special location to interrupt another processor. The other processor reads the message from the receiving buffer and acknowledges the interrupt by resetting the flag. Likewise for transmission of data the other direction, the second processor writes to the transmission buffer and sets another flag in a special location to to interrupt the first processor. The first processor reads the data from the transmission buffer and resets the flag. If a memory contention situation occurs, the lower priority microprocessor has one or more wait states inserted until access is available. reversed location

The GSC Controller section also interfaces with an RS-232 port 324, as does the motion controller at 326. The peripheral controller has an RS-422 port shown at 328 instead of the RS-232 port.

Fig. 11 shows in more detail at 300 the GSC communication portion of the device control board 106. As brought out above the section utilizes the Intel 80C152 processor 350 to communicate information from the GSC board of the System Controller to shared memories 320 and 322 (memory 322 is shown only in outline). The operation is similar to that already described for the GSC board and will not be further discussed here.

Fig. 12 is a block diagram of the motion and/or peripheral controller section 302 and 304, each of which preferably comprises similar functional blocks using similar parts. Since the sections are similar only the motion control section will be described. This section includes

three major components: control processor 360, preferably Intel 80C196KC based, for executing all motion control associated software; address-decoding logic shown at 362 for demultiplexing the CPU address from the address/data bus and for enabling the proper memory device for accessing; and the memory block shown generally at 364 comprising EPROM 366, preferably 64K bytes for code storage, SRAM 368 for data storage, and three, suitably 1K-byte dual port SRAM's 370, 372 and 374, respectively, for message buffers.

The motion control processor performs several software controlled functions. It generates motion profiles, preferably based on the function profiles which are downloaded from the system controller. It monitors encoder feedback and sensor data from the Peripheral Control Processor of section 304 and processes this information to control devices such as motors and sensors (not shown in this Figure) via the GPSL link described below. It preferably executes a user selected digital filter algorithm to generate pulse-width-modulated (PWM) control commands for servo motors. It will also generate half-step pulse commands for open-loop step motors and will notify the System Controller when any error condition occurs.

As mentioned previously, the peripheral control block comprises the same functional blocks as described above for the motion controller. The processor in block 304 will execute module function profiles which are preferably downloaded from the System Controller and will control or interface with I/O boards via the GPSL link.

The GPSL link of which the Master controllers 306 and 308 form a portion provides a cyclic, preferably 500K Baud, master-slave serial communication which is optimized for motion control protocol. Each master controller is suitably implemented in a programmable logic device (PLD). Further details of the GPSL link are available from Application S.N. _____, (Atty. Docket E-162) entitled Improved Communication Link for Control Applications filed on even date herewith, assigned to the assignee of the instant

application and specifically incorporated herein by reference.

In accordance with the protocol for this communication link, each GPSL frame has one "flag" byte followed by eight (8) data channels, each data channel having three (3) bytes. Each data byte preferably comprises ten (10) bits, including eight (8) data bits, one (1) odd-parity bit and one zero-insertion" bit. Each data bit is preferably 8X oversampled.

The controllers perform the following functions. As a master node they generate a "flag" field as reference to synchronize all Slave nodes. They fetch outgoing data from shared memory and pack it in proper format to send out. They unpack incoming data and place it in the shared memory's receive buffers.

Fig. 13 is a block diagram showing a GPSL control link arrangement. The device controller 106 has two communication ports, only one of which is illustrated in Fig. 13, for example 312, for connecting to a plurality of up to eight devices each, some of which are illustrated at blocks 400, 402 and 404 . Each GPSL master node is connected to up to eight slave nodes, 406, 408, 410 each communicating to its respective device and with the serial communication port 312 at respective communication ports 412, 414, and 416. The details of these blocks are shown in Application S.N. _____, (Atty. Docket E-162) entitled Improved Communication Link for Control Applications previously incorporated by reference and will not be further described here. The physical connection of the GPSL link is preferably implemented by two half-duplex RS-485 multipoint links. Four wire telephone cables shown at 420, 422, 424, and 426 are suitable for carrying these two pairs of differential signals, which swing between 0V and +5V. Modular phone jacks (not shown) are suitable for connector receptacles.

For best results in accordance with the invention the device controller interfaces with determined motors via a universal motor drive board such as the one illustrated at

500 in the block diagram of Fig. 14. It will be understood that the board 500 is representative of the ones shown at 108 and 110 of Fig. 5. The illustrated board 500 is a fully digital control, versatile motor driver which can drive a wide range of motors . When these boards are used in conjunction with the serial link described above and in application S.N. _____, (Atty. Docket E-162), it will be appreciated that system integration time can be significantly reduced and system reliability increased. The significant features are a universal commutation control which can drive open- or closed-loop stepper motors, or DC or brushless motors. The board includes built-in quadrature-decoding circuitry for conventional optical encoders. The board also includes built-in "commutation phase advance" circuitry to improve high-speed performance and a built-in pulse-width-modulation (PWM) generator.

Turning now to Fig. 14, the board 500 comprises a slave node 502 of the GPSL link associated with internal registers illustrated at 504. The board 500 also includes position decoder/phase advance logic shown at 506, universal commutation logic illustrated at 508 and PWM generator 510 for control of the power switching stage 512 by the power drive control block 514. The drive board is shown outputting drive information to representative motor 516 which in accordance with the invention may be a DC, DC-brushless or stepper motor. The rotor shaft position may be monitored by means of encoder 518.

The GPSL block 502 provides the control link between the motor driver such as 500 and its associated device controller such as the device 106 of Fig. 10. The basic functions of this block to receive the motor commands and other control signals from the device controller. It provides frame synchronization with the master node of the device controller, receives information from the controller, checks the information and latches the commands and control data into the internal registers 504 and the decoder block 506. It also collects and formats the data and drive status for transmittal to the device controller.

Fig. 15 is a block diagram of the position decoder 506. The encoder information is fed to digital filter 550 and from there to decoding logic section 552 to provide a count and direction information to 16-bit up/down counter 554 for providing current position information to memory registers (not shown) which information is transmitted back to the device controller via the GPSL node 502. The input from the encoder may include polarity switch 556.

Suitably, a velocity signal output is provide to the universal commutation logic board. As illustrated the last position output is stored in a last position buffer means 558 and subtracted from the current position data at subtracter 560. Preferably diagnostic inputs such as a 12.5KHz clock input and other diagnostic signals as desired in diagnostic section 562.

The heart of the motor drive is a universal commutation logic. Fig. 16 is a block diagram of a suitable logic in accordance with the invention. As shown generally at 508, the logic section comprises a look-up table stored in EPROM block 600 which may include a plurality of varied commutation sequences such as , for example, half-step open-loop stepper motor, full-step closed-loop stepper motor, DC brush motor, and DC brushless motor commutation sequences.

Position encoder information as described in connection with Fig. 15, is received at the counters shown here at 602 and 604. As seen in Fig. 16, offsets may be added in via an offset switch 606 at a ten bit adder 608. The motor type setting and the motor shaft position are read and the proper sequence is selected from the look-up tables automatically.

When the motor speed increases, the phase angle between the winding current in the motor and the commutation window shifts away. This phase shift reduces the usable motor torque. It has been found to be desirable to to compensate for this phase shift for high-speed applications. In Fig. 5 in accordance with the invention, there is provided a programmable phase advance look-up table in EPROM

610 from whence in correspondence with the motor velocity, a determined phase advance is obtained which may be added to the position and offset information at adder 608. The resulting output is provided via 4-bit MUX 612 to the commutation sequence block 600 for controlling the power drive illustrated in Fig. 17.

Returning to Fig. 14, the PWM generator 510 converts the received digital command into an analog pulse train, suitably 32 KHz, to modulate in conventional manner the motor current and motor speed.

The power switching stage is illustrated in the block diagram of Fig. 17. As shown, the block 512 comprises two major components. There are two pairs of H-bridge power switches, one of which is shown generally at 650, the others being shown only in outline. For best results they should be capable of delivering 1000 watts output. The other component is current-limiting circuitry shown generally at 652. Preferably, the current limit may be set by the user. Then as soon as any over-current condition is detected at the power switch, the PWM is disabled almost instantaneously. Conveniently, the prohibition is removed at the next PWM clock edge and the protection circuit restarted.

For further protection, as seen in Fig. 16, whenever the PWM command changes direction, there is a short commutation gap provided at 660 to prevent switch "shoot-through." It has also been found that protection is enhanced if when any communication error is detected, all drivers are turned off. When the driver has to be reset for any reason, the driver will stay in its idle state until the device control unlocks the condition.

CLAIMS

1. A system electrical architecture comprising control means for controlling a plurality of determined devices chosen from the group consisting of stepper motors, DC motors and brushless DC motors, said control means communicating with at least one motor drive controller by means of a master-slave communication means, said motor drive controller being operative for controlling at least a selected one of said plurality of devices, said master-slave communication means being a serial communication means, said control means including means for receiving and storing control parameters for operation of said plurality of devices, and said means for receiving being a second communication means adapted for communication with a system control means.

2. The system architecture of claim 1 wherein the second communication means is a GSC communication means.

3. The system architecture of claim 1 further comprising a second master-slave communication means for communication with at least one I/O means, said I/O means being connected to control at least one peripheral device.

4. The system architecture of claim 1 wherein the motor drive controller is a universal drive controller operative to selectively control each of said plurality of determined devices.

5. A system electronic architecture comprising a system control means for commanding operation of a plurality of devices, a first communication means, said system control means communicating via said first communication means with at least one device control means for controlling a plurality of determined devices chosen from the group consisting of stepper motors, DC motors and brushless DC

motors, said device control means communicating with at least one motor drive controller by means of a master-slave communication means, said motor drive controller being operative for controlling at least a selected one of said plurality of devices, said master-slave communication means being a serial communication means, said device control means including means for receiving data from the system control means via said first communication means and for storing control parameters for operation of said at least selected one of the plurality of devices.

6. The system architecture of claim 5 wherein the second communication means is a GSC communication means.

7. The system architecture of claim 5 further comprising a second master-slave communication means for communication with at least one I/O means, said I/O means being connected to control at least one peripheral device.

8. The system architecture of claim 5 wherein the motor drive controller is a universal drive controller operative to selectively control each of said plurality of determined devices.

9. The architecture of claim 8 further comprising phase advance compensation means for providing a phase advance input for compensation for motor speed.

10. In a system architecture including a control means for controlling motor operation, the improvement comprising a universal motor drive apparatus including means for receiving motor commands from said control means, means for decoding encoder positioning information, commutation logic means, said commutation logic means storing commutation information for determined motor types, meams for accessing the commutation information in accordance with commands from the control means, pulse width modulation generator means, power switching means and power drive control means

connected to said power switching means, said power drive control means controlling said power switching means for driving a selected one of said motor types in accordance with information received from a selected one of said commuation means and said pulse width generator means.

11. The architecture of claim 10 further comprising phase advance compensation means for providing a phase advance input for controlling the power drive control for compensation for motor speed.

12. The architecture of claim 10 wherein the commutation logic means includes EPROM means for storing the commutation information.

13. A system electrical architecture substantially as herein described with reference to and as illustrated in the accompanying drawings.

14. Any novel combination or sub-combination of features disclosed and/or illustrated herein.

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Examiner's report to the Comptroller under Section 17
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Databases (see below)
(i) UK Patent Office collections of GB, EP, WO and US patent specifications.

(ii) ONLINE DATABASES: WPI

Documents considered relevant following a search in respect of Claims :-
1 TO 9

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages		Relevant to claim(s)
X, Y	GB 2261750 A	(HONDA) see Figures 1 and 2 and page 7 line 18 to page 8 line 6 in particular	X: 1, 5 Y: 2
X, Y	GB 2132382 A	(TRUTZSCHLER GMBH) whole document	X: 1, 5 Y: 2
X, Y	EP 0272397 A2	(VICKERS) see Figure 1 and column 3 lines 6 to 26	X: 1, 3, 5, 7 Y: 2
Y	US 4780814	(HAYEK) whole document	2

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